Notice of Allowability	Application No.	Applicant(s)	
	09/882,328	LI, SHUO-YEN ROBERT	
	Examiner	Art Unit	
	John Pezzlo	2662	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *amendment filed 11 September 2001*.

2. ☒ The allowed claim(s) is/are *4-22 (renumbered 1-19)*.

3. ☒ The drawings filed on *15 June 2001* are accepted by the Examiner.

4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

6. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☒ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date 15 June 2001
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

JOHN PEZZLO
PRIMARY EXAMINER

DETAILED ACTION

Allowable Subject Matter

Claims 4-22 are allowable over the prior art of record.

Reasons for Allowance

The following is an examiner's statement of reasons for allowance:

Applicant has claimed the following uniquely distinct features in the instant invention, which are not found in the prior art, either singularly or in combination:

1. Regarding claim 4 - A method for self-routing a packet through a $b2^n x b2^n$ switching network comprising configuring the switching network with (a) 2^n output groups, each of the output groups having a distinct binary address in the form of $b_1 b_2 \ldots b_n$ with b indistinguishable output ports, and (b) k super-stages of concentrators wherein each of the concentrators is a 2bx2b partial sorting network of interconnected routing cells and b of its 2b output ports are grouped into a 0-output group while the remaining b output ports are grouped into a l-output group, the network being characterized by the guide y(1), y(2), . .. , y(k), where y is a mapping from the set {1, 2, .. . , k} to the set {1, 2, .. . , n}, and wherein the packet is either a real data packet destined for the output group at the binary destination address $d_1 d_2 \ldots d_n$, or an idle packet having no pre-determined destination, generating a routing tag $1 d_{y(1)} d_{y(2)} \ldots d_{y(k)}$ for the real data packet with reference to the guide of the network and the destination address of the packet, and routing the

real data packet through the network by using $ld_{y(j)}$ in the routing tag in the j-th super-stage concentrator, $l \leq j \leq k$, to select between the O-output group or the l-output group of the j-th super-stage concentrator to emit the real data packet.

2. Regarding claim 5 – A method for self-routing a packet through a $b2^n x b2^n$ switching network, the network: including 2^n output groups, each of the output groups having a distinct binary address in the form of $b_1 b_2 \ldots b_n$ with b indistinguishable output ports, and k super-stages of concentrators wherein each of the concentrators is a 2bx2b partial sorting network of interconnected routing cells and b of its 2b output ports are grouped into a 0-output group while the remaining b output ports are grouped into a l-output group, and being characterized by the guide y(1), y(2), ... , y(k), where y is a mapping from the set {1, 2, . . . , k} to the set {1, 2, . . . , n} , and wherein the packet is either a real data packet destined for the output group at the binary destination address $d_1 d_2 \ldots d_n$, or an idle packet having no pre-determined destination, the method comprising generating the routing tag $1d_{y(1)}d_{y(2)} \ldots d_{y(k)}$ for the real data packet with reference to the guide of the network and the destination address of the packet, and routing the real data packet through the network by using $ld_{y(j)}$ in the routing tag in the j-th super-stage concentrator, $l \leq j \leq k$, to select between the 0-output group or the l-output group of the j-th super-stage concentrator to emit the real data packet.

3. Regarding claim 6 – A method for self-routing a plurality of real data packets through a $b2^n x b2^n$ switching network, the switching network being characterized by the guide y(1), y(2), . . . , y(k) where y is a mapping from the set {1, 2. .. . , k} to the set {1, 2, .. . , n}, and having (a) $b2^n$ external input ports, (b) 2^n output groups, each of the output groups having a distinct binary address in the form of $b_1 b_2 \ldots b_n$ with b indistinguishable output ports, and (c) k super-stages of

2b-to-b concentrators wherein each of the concentrators is a 2bx2b partial sorting network of interconnected routing cells where each of the routing cells is a sorting cell associated with the partial order "10 ('0-bound') < 00 ('idle') < 11 ('1- bound')", b of the 2b output ports of each of the concentrators are grouped into a 0-output group while the remaining b output ports are grouped into a l-output group, and extra circuitry arranged at the output end of each of the concentrators wherein the extra circuitry is composed of 2b parallel lxl switching elements, one at each of the output ports of the concentrator, and each of the real data packets arriving at a distinct external input port determining an active input port and destined for an output group at the binary destination address $d_1d_2 \ldots d_n$, the method comprising generating an idle packet as a stream of '0' bits at each of the non-active external input ports, generating a routing tag $1d_{y(1)}d_{y(2)} \ldots d_{y(k)}$ for each of the real data packets with reference to the guide of the network and the destination address of the packet, generating a routing tag which is a string of k+1 '0' bits for each of the idle packets, routing the real data packets and the idle packets through the network by sorting the packets by the 2b-to-b concentrators of the network, wherein the sorting at each of the concentrators includes the sorting at each of the sorting cells of the concentrator such that the sorting is with respect to the associated partial order and is based upon the leading two bits, which are either '10' or '11' for a real data packet, or '00' for an idle packet, of the routing tag of each of the two packets arrived at each of the sorting cells, and processing the routing tag of each of the packets by the extra circuitry at the output end of the concentrator before the said each of the packets exits from the j-th super-stage concentrator by removing the second leading bit from the routing tag or rotating the second leading bit to the end of the routing tag such that the

leading two bits of the routing tag of each of the packets at each of the j-th super-stage concentrators, $1 \le j \le k$, are always '$1d_{y(j)}$' or '00' .

4. Regarding claim 14 – A system for self-routing a packet comprising a $b2^n x b2^n$ switching network, the switching network having (a) 2^n output groups, each of the output groups having a distinct binary address in the form of $b_1 b_2 \ldots b_n$ with b indistinguishable output ports, and (b) k super-stages of concentrators wherein each of the concentrators is a 2bx2b partial sorting network of interconnected routing cells and b of its 2b output ports are grouped into a 0-output group while the remaining b output ports are grouped into a 1-output group, the network being characterized by the guide y(1), y(2), .. . , y(k), where y is a mapping from the set {1, 2, ... , k} to the set {1, 2, ... , n}, and wherein the packet is either a real data packet destined for the output group at the binary destination address $d_1 d_2 \ldots d_n$, or an idle packet having no pre-determined destination, routing tag circuitry for generating a routing tag $1d_{y(1)}d_{y(2)} \ldots d_{y(k)}$ for the real data packet with reference to the guide of the network and the destination address of the packet, and routing control circuitry for routing the real data packet through the network by using $1d_{y(j)}$ in the routing tag in the j-th super-stage concentrator, $1 \le j \le k$, to select between the 0-output group or the 1-output group of the j-th super-stage concentrator to emit the real data packet.

5. Regarding claim 15 - A system for self-routing a plurality of real data packets comprising a $b2^n x b2^n$ switching network having a plurality of 2b-to-b concentrators interconnected into a k-stage bit-permuting network characterized by guide y(1), y(2), . . . , y(k) where y is a mapping from the set {1, 2, . .. , k} to the set {1, 2, ... , n}, and having (a) $b2^n$ external input ports, (b) 2^n output groups, each of the output groups having a distinct binary address in the form of $b_1 b_2 \ldots b_n$ with b indistinguishable output ports, and (c) k super-stages of 2b-to-b concentrators wherein

each of the concentrators is a 2bx2b partial sorting network of interconnected routing cells where each of the routing cells is a sorting cell associated with the partial order "10 ('0-bound') < 00 ('idle') < 11 ('1- bound')", b of the 2b output ports of each of the concentrators are grouped into a 0-output group while the remaining b output ports are grouped into a l-output group, and extra circuitry arranged at the output end of each of the concentrators wherein the extra circuitry is composed of 2b parallel lxl switching elements, one at each of the output ports of the concentrator, and wherein each of the real data packets arrives at a distinct external input port and is destined for an output group at the binary destination address $d_1d_2...d_n$, idle-packet-generating circuitry, coupled to the external input ports, for generating an idle packet as a stream of '0' bits at each of the external input ports of the switching network if no real data packet arrived at that external input port, routing tag circuitry, coupled to the external input ports, for generating a routing tag $1d_{y(1)}d_{y(2)}...d_{y(k)}$ for each of the real data packets with reference to the guide of the network and the destination address of the packet, or generating a routing tag which is a string of k+1 '0' bits for each of the idle packets, routing control circuitry, coupled to the concentrators, for routing the real data packets and the idle packets through the network by sorting the packets by the 2b-to- b concentrators of the network, wherein the sorting at each of the concentrators includes the sorting at each of the sorting cells of the concentrator where the sorting is with respect to the associated partial order and is based upon the leading two bits, which are either '10' or '11' for a real data packet, or '00' for an idle packet, of the routing tag of each of the two packets arrived at the cell, and extra circuitry at the output end of the j-th super-stage concentrator, $l \leq j \leq k$, for processing the routing tag of each of the packets before the said each of the packets exits from the j-th super-stage concentrator by removing the second leading

bit from the routing tag or rotating the second leading bit to the end of the routing tag such that the leading two bits of the routing tag of each of the packets at each of the j-th super-stage concentrators, $l \leq j \leq k$, are always '$ld_{y(j)}$' or '00'.

The closest prior art, either singularly or in combination, fail to anticipate or render the above limitations obvious.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

Claims 4-22 being allowable, **Prosecution On The Merits Is Closed** in this application.

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

1. Kamaraj et al. (US 6,501,757 B1) discloses an ATM switch.

2. Yang et al. (US 5,940,389) discloses an enhanced partially self-routing algorithm for controller Benes networks.

3. Szymanski, "Design Principles for Practical Self-Routing Nonblocking Switching Networks with 0(NlogN) Bit-Complexity", IEEE, 17 May 1997, pages 1057-1069.

4. Szymanski, "Randomized Routing of Virtual Connections in Essentially Nonblocking Log N-Depth Networks, IEEE, 15 February 1994, pages 2521-2531.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to John Pezzlo whose telephone number is (571) 272-3090. The examiner can normally be reached on Monday to Friday from 8:30 AM to 4:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hassan Kizou, can be reached on (571) 272-3088. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (571) 272-2600.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C.

or faxed to:

(703) 872-9306

For informal or draft communications, please label ?PROPOSED≅ or ?DRAFT≅

Hand delivered responses should be brought to:

Jefferson Building

500 Dulany Street

Alexandria, VA.

John Pezzlo

23 June 2005

JOHN PEZZLO
PRIMARY EXAMINER